REMARKS

By this amendment, applicants have amended the specification to correct typographical and idiomatic errors. Applicants have also amended the claims to more clearly define their invention. In particular, claim 1 has been amended to clarify the preamble and the steps of the method. Claim 1 has also been amended to indicate that the substrate has an insulation layer provided thereon, that the insulation layer has a hole formed therein, and that the bottom electrode is formed on at least a side wall of the insulation layer in the hole. See, e.g., example 1 at page 15, line 5 et. seq. of applicants' substitute specification. Claim 2 has been amended to clarify that the ratio represents a volume ratio. This amendment is supported by the description at, e.g., page 16, lines 3 - 7 of the substitute specification wherein it is indicated that the reaction gas and carrier gas are introduced in an amount measured in "sccm." As noted by the attached United States Patent No. 6,342,452, "sccm" denotes standard cubic centimeters per minute and, therefore, clearly refers to volume. Claim 8 has been amended to depend from claim 1 or 2 and to indicate that the cyclopentadienyl complex is dissolved in an organic solvent having a solubility for the starting precursor of 0.05 mol/l or more. See, e.g., page 11, lines 15 - 17, of applicants' substitute specification.

Applicants have also added claims 15 - 17 to define further aspects of the present invention. Claim 15 is supported by the disclosure at, e.g., page 17, lines 8 - 9 of applicants' substitute specification; claim 16 is supported by, e.g., page 9, lines 10 - 14 of applicants' substitute specification; and claim 17 is supported by, e.g., page 7, lines 1 - 6 of applicants' substitute specification.

In view of the foregoing amendments to claims 1, 2 and 8, reconsideration and

withdrawal of the objection to claims 1 and 8 on page 2 of the office action and the rejection of claim 2 under 35 USC 112, second paragraph, on page 3 of the office action are requested.

Claims 1, 2, 5, 8, 9 and 12 stand rejected under 35 USC 103(a) as allegedly being unpatentable over United States Patent No. 5,973,351 to Kotecki et al in view of United States Patent No. 5,130,172 to Hicks et al. Applicants traverse this rejection and request reconsideration thereof.

The elected invention relates to a method of manufacturing a semiconductor device having a dielectric capacitor including a bottom electrode, a dielectric layer and a top electrode on an underlying substrate having a three-dimensional structure. According to the present invention, the dielectric capacitor is provided on a substrate that has an insulation provided thereon, the insulation layer having a hole formed therein. See, e.g., Figure 4. According to the present invention, the bottom electrode is formed on at least a side wall of the insulation layer in the hole. The dielectric layer is provided on the bottom layer and the top electrode is provided on the dielectric layer. Applicants have found that by forming the bottom electrode and the top electrode by a metalorganic chemical vapor deposition process at 180°C or higher and 250°C or lower using a cyclopentadienyl complex as a precursor, homogenous electrode layers can be provided, even on the side wall of the insulation layer in the hole. Such is neither disclosed nor suggested by Kotecki et al and Hicks et al.

The patent to Kotecki et al discloses a semiconductor device having a capacitor containing an insulator material having a high dielectric constant and high storing capability. It is disclosed that the bottom and top electrodes can be formed of

conventional materials, such as Pt, Ir, Ru, noble metals, conductive oxides of noble metals, or conductive nitrides and oxides. As recognized by the Examiner, this patent does not disclose the method of the present invention, including forming the bottom and top electrodes by a metalorganic chemical vapor deposition process at 180°C or higher and 250°C or lower using a cyclopentadienyl complex as a precursor. Moreover, the Kotecki et al patent does not disclose forming the bottom electrode on at least a side wall of an insulation layer in a hole on the substrate.

The patent to Hicks et al discloses a process for coating metal on a substrate. The process uses organometallic compounds in the presence of a reducing fluid to produce high purity films capable of selective deposition on substrates containing, for example, tungsten and silicon. The films are deposited using chemical vapor deposition or gas phase deposition. However, the Hicks et al patent also does not disclose forming the bottom electrode on at least a side wall of an insulation layer in a hole on the substrate. Thus, the Hicks et al patent does not remedy a basic deficiency of Kotecki et al. Therefore, even the combination of Kotecki et al and Hicks et al would not have suggested the presently claimed invention.

Moreover, applicants traverse the conclusion of the Examiner that "[t]he selection of the ratio of the gases and the solubility of the precursor in the solvent is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species." It is submitted the Examiner has not supported this conclusion with the evidence required to support a rejection under 35 USC 103.

In addition, while the Hicks et al patent discloses the use of various organo-

metallic compounds in the presence of a reducing fluid at various temperatures, it is submitted this patent does not specifically suggest the formation of a bottom electrode and top electrode at a temperature between 180° and 250°C using a cyclopentadienyl complex as a precursor, the bottom electrode being formed on at least a side wall of an insulation layer in a hole in the insulation layer. Applicants have found that the adhesion rate of the complex is fairly constant in the temperature range between 180 and 250°C, while the decomposition/adhesion on the surface proceeds preferentially at higher temperatures. Thus, the present invention provides a process for manufacturing a semiconductor device having a dielectric capacitor on an underlying substrate having a three-dimensional structure (i.e., a process including forming a bottom electrode on at least a side wall of the insulation layer on the hole). Such a method is neither disclosed nor suggested by Kotecki et al or Hicks et al, or even by the combination thereof.

For the foregoing reasons, it is submitted the presently claimed invention is patentable over the proposed combination of Kotecki et al and Hicks et al.

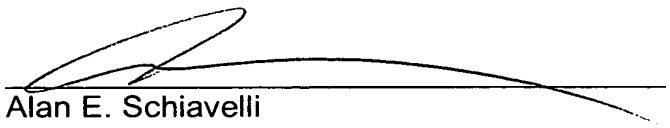
In view of the foregoing amendments and remarks, favorable reconsideration and allowance of all of the claims now in the application are requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry,

Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 501.39983X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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